International Journal of Electrical and Electronics Engineering (IJEEE)
ISSN 2278-9944
Vol. 2, Issue 4, Sep 2013, 57-62

International Academy of Science, Engineering and Technology
Connecting Researchers; Nurturing Innovations

DESIGN OF A CCII-BASED PIPELINE A/D CONVERTER

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ABSTRACT

Nowadays electronic applications, including wireless communication, imaging and video, demand high-resolution and low-distortion analog-to-digital conversion (ADC) with a signal bandwidth of tens of MHz. This paper reports a design of a pipeline ADC using second-generation current conveyor (CCII) and this used CCII is based on CMOS inverter. Simulation is done in cadence environment with 0.18 µm technology using Virtuoso simulator. Simulation results are reported that shows the capability and effectiveness of the proposed design. Authors have verified the capability of this design to operate over the high frequency range (10 to 100MHz). Best simulation results obtained on cadence environment with 180nm technology. Also the layout design is carried out and verified the performance of the proposed 10 bit ADC design. Finally a result of complete ADC design is reported and compared with earlier reported work. This design will be beneficial for young designers and manufacturers.

KEYWORDS: Pipelined ADC, Current Conveyor, Cadence, CMOS Inverter and Resolution

INTRODUCTION

The pipeline ADC architecture is used for many applications because it achieves both high resolution and high speed. Very high dynamic range ADCs can simplify system design, reduce overall cost, and maximize receiver sensitivity. Design of these ADCs presents difficult architectural tradeoffs. A great deal of research has been done in the industry and at the university level to understand these tradeoffs and find alternative design techniques [1]-[3]. Furthermore, aggressive device scaling in modern CMOS technology, coupled with low supply voltage operation, has made the design of op-amps difficult. Analog-to-digital converters (ADCs) are key components in digital communication receivers. For wideband applications, an ADC resolution of 8 or 9 bits is sufficient to meet the system signal-to-noise ratio (SNR) requirement [4]. However, a sampling rate of hundreds of M sample/sec. is required to support the increasing signal bandwidth and to relax the anti-alias filter design. In addition, the power consumption of ADCs has to be minimized for the portable operation powered by battery.

PIPELINE-ADC ARCHITECTURE

A second generation current conveyor (CCII+) is given in figure 1 and its basic principle is shown in figure 2. Generally pipeline ADCs are designed using OPAMPs. The continuing trend of submicron CMOS technology scaling, which is coupled with lower power supply. At low power supply for OPAMP and speed. Large open loop gain is difficult to achieve without sacrificing bandwidth.

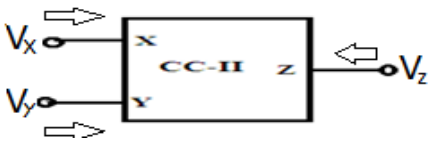
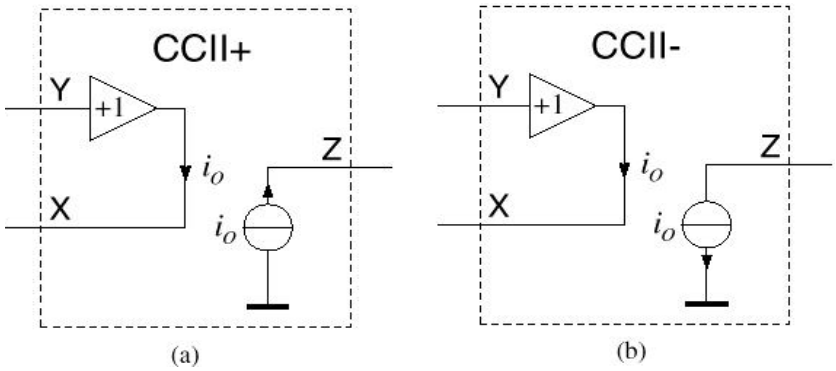


Figure 1: Second Generation Current Conveyor

Second Generation Current Conveyor (CCII) - In first generation current-conveyor only one of the virtual grounds in terminals X and Y is used and the unused terminal must be grounded or otherwise connected to a suitable potential. This grounding plays an important role in many applications it must be done carefully since a poorly grounded input terminal may cause unwanted negative impedance at the other input terminal. More- over, for many applications a high impedance input terminal is preferable. For these reasons, the second generation current-conveyor was developed. It has one high and one low impedance input rather than the two low impedance inputs of the CCI [5]-[7].



The Positive Conveyor CCII+, $i_z = i_x$ **The Negative Conveyor CCII-, $i_z = -i_x$**

Figure 2: The Principle of the Second Generation Current- Conveyors

The Y-terminal of the second generation current conveyor is a voltage input and the Z-terminal is a current output, the X-terminal can be used both as a voltage output and as a current input. Therefore, this conveyor can easily be used to process both current and voltage signals unlike the first generation current-conveyor or the operational amplifier. Figure 3 represents a schematic design of CCII and Matrix representation of CCII is given as:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \Rightarrow \quad \begin{aligned} i_y &= 0 \\ v_x &= v_y \\ i_z &= \pm i_x \end{aligned}$$

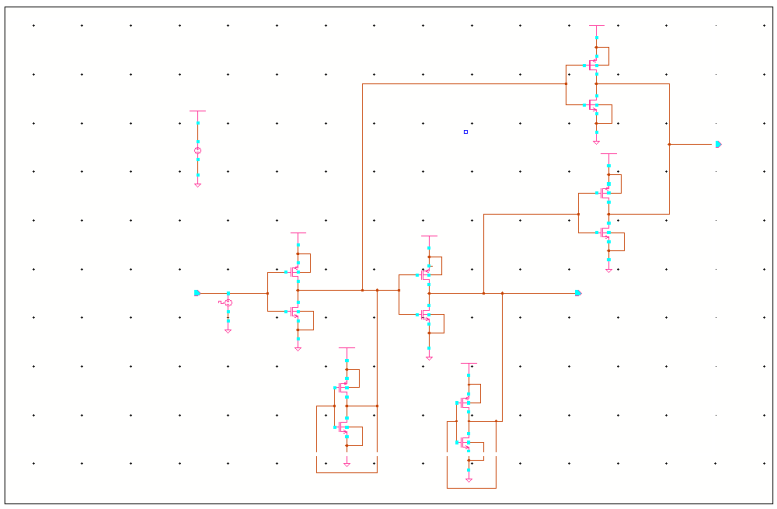


Figure 3: Schematic Design View of CCII

DESIGN OF A 10-BIT PIPELINE ADC

This design is combination of 10 stages, each stage provide one bit output. Each stage contains sample and hold, comparator and 1-bit MDAC. Comparator provides digital output which is final output of the perticular stage. In this design authors have implemnted MDAC using transmission gate and CCII. Figure 4 has given first stage of the proposed ADC design and figure 5 shows the complete design of 10 bit pipeline ADC.

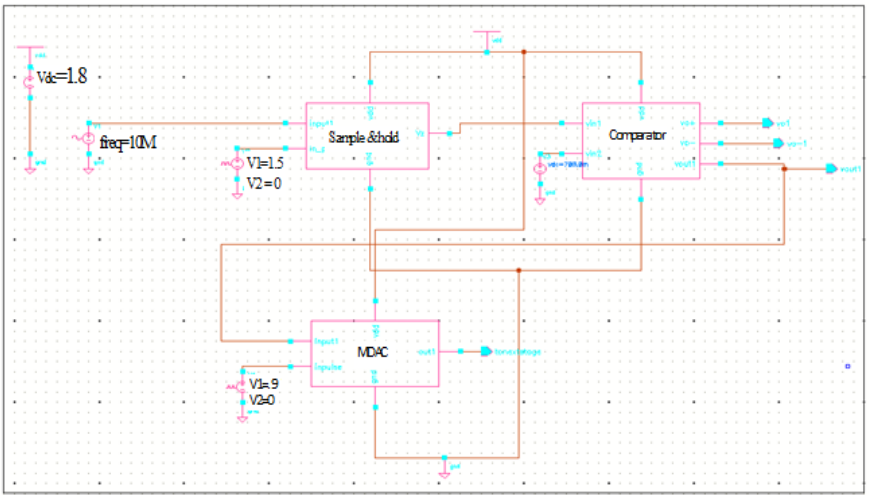


Figure 4: A Propoesd 10-Bit Pipeline ADC

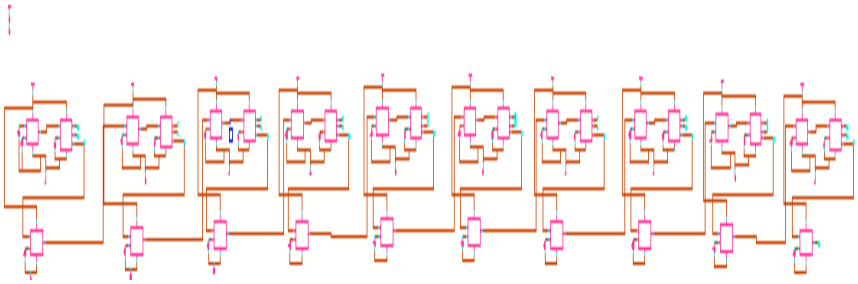


Figure 5: Complete Design of a Propoesd 10-Bit Pipeline ADC

Figure 6 and 7 shows the layout of inverter based current conveyor and the layout of 10-bit Pipeline ADC respectively.

SIMULATION RESULTS

Finally 10 bit pipeline ADC is designed and simulated in cadence environment with 0.18µm technology. Figure 8 shows the transient response of MDAC and figure 9 shows the complete 10 bit pipeline ADC output for the exponential input of 1.8V. The complete circuit has the power dissipation is 6.33 mW. Authors have also simulated this design with software based implemented algorithm and determined parameters like DNL, INL, SINAD and ENOB as given in table. Table 1 shows various measured parameters with comparison of earlier reported work.

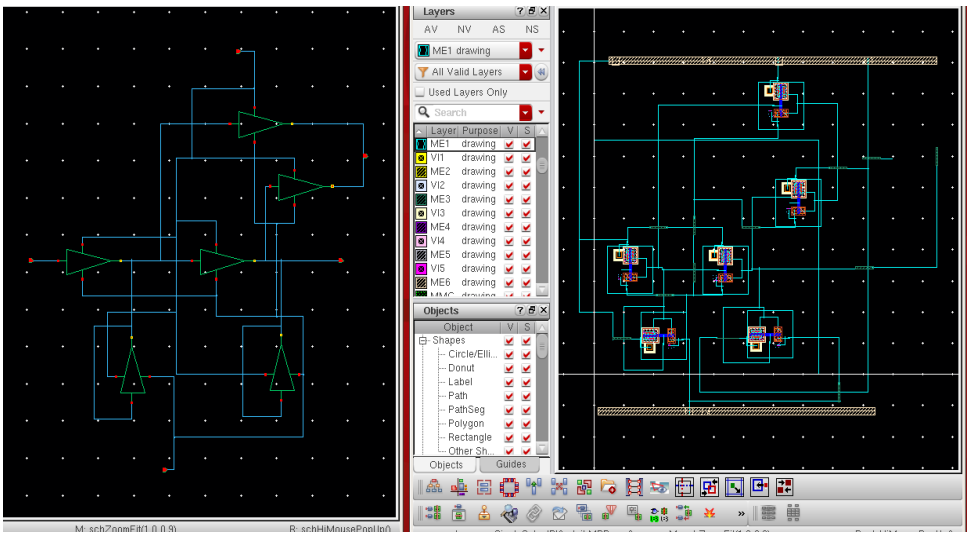


Figure 6: The Layout of Inverter Based Current Conveyor

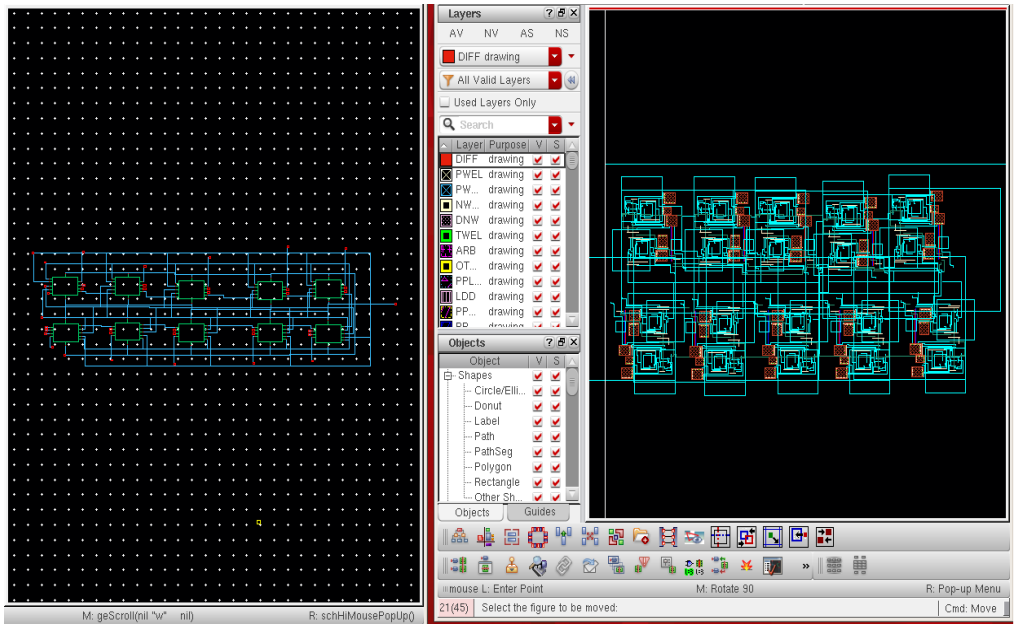


Figure 7: The Layout of 10-Bit Pipeline ADC

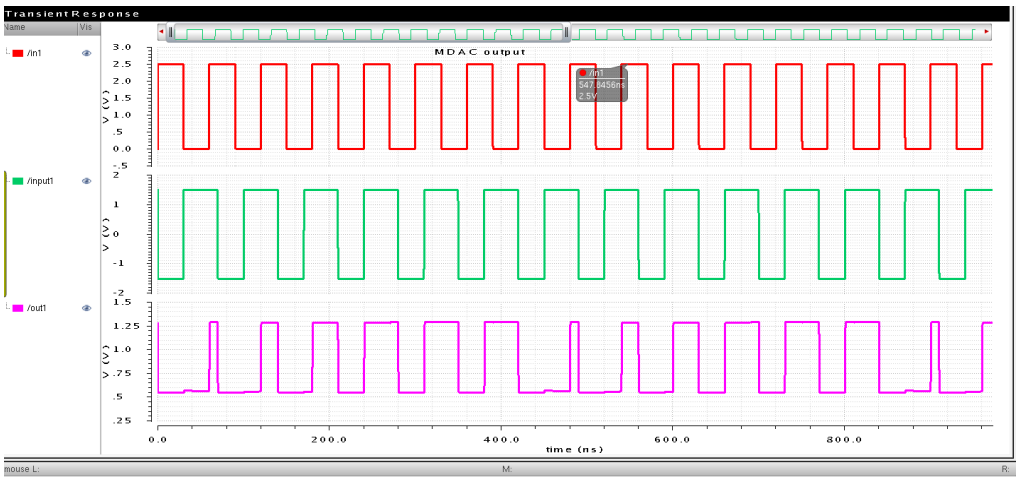


Figure 8: Transient Response of MDAC

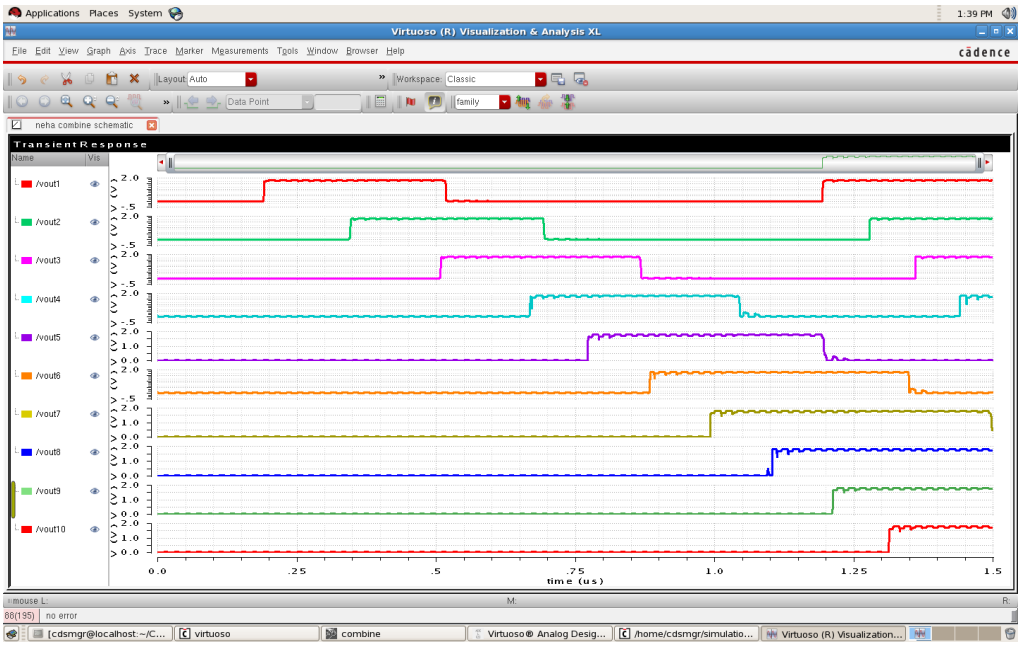


Figure 9: Complete 10 Bit Pipeline ADC Output

Table 1: Final Results of a Proposed 10 Bit Pipeline ADC

Parameter	Used Parameter Values	Measured/Estimated Parameters	Ref. [12] Values for 8 Bit	Measured/Estimated Values with Proposed Design for 10 Bit with 30000 Samples
Technology	0.18 um CMOS	Power dissipation	14.2 mw	6.63 mw
Power Supply	1.8 V	Area	1.12 mm^2	0.66 mm^2
Sampling frequency	25MHz	Effective number of bits	7.66 bits for 8 bit	9.48 Bits with 30 MHz for 10 bit
Determined ADC parameters		SINAD	47.8932 dB for 8 bit	58.82 dB for 10-bit
		$(S/N)_{ideal}$	49.92 db for 8 bit	
		INL	1.2 LSB for 8 bit	0.98 LSB for 10 bit
		DNL	0.82 LSB for 8 bit	0.87 LSB for 10 bit

CONCLUSIONS

The proposed architecture is implemented in a 180nm digital CMOS technology with standard threshold voltage devices only. The presented pipelined ADC design is compact in size as compared with other ADCs with similar sampling rates and resolutions. A low-voltage CMOS positive type second generation current conveyor based 10-pipeline ADC introduced in this paper. CCII based pipeline ADC has major advantages in terms of linearity, noise and power and also good noise performance.

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